

**CUSTOMER NO.: 24498**

**Application No. 10/083,011**

**Reply to Office Action of Aug. 24, 2004**

**Response dated: January 6, 2005**

**Attorney Docket No. PF010024**

**Remarks/Arguments**

Claims 1 – 8 are pending in this application with claims 1, 2, 4 and 6 – 8 are being amended. New claims 9 – 11 are added for consideration and claim 3 is cancelled by this response. Support for the amendments to claims 1, 2, 4 and 6 - 8 can be found throughout the specification and specifically on page 2, line 28 through page 6, line 3. Similarly, support for new claims 9 – 11 can also be found in the above identified passages of the present specification. Thus, it is respectfully submitted that no new matter has been added by either the amendments to claims 1, 2, 4 and 6 – 8 or new claims 9 – 11.

**Rejection of Claims 1-8 under 35 USC § 102**

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Cottle, et al., (U.S. Patent No. 6,263,396).

The present claimed invention recites a video apparatus with a digital decoder and method for controlling the video apparatus. The apparatus includes a first memory for storing video data and a second memory for storing on-screen display data. An on-screen display circuit generates on-screen display graphics signal from the on-screen display data in the second memory. The first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and to transfer the on-screen display data back to the second memory in response to a request for display of data stored in the first memory.

Cottle et al. disclose a programmable interrupt controller for a single interrupt architecture processor including a plurality of interrupt sources each operable to generate an interrupt. A dynamically alterable interrupt mask selectively blocks

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interrupt signals for the interrupt sources. Interrupts permitted by the dynamically alterable interrupt mask are processed by an interrupt handler for the single interrupt architecture processor in order of priority. In addition, processing for a lower priority interrupt is interrupted in order to process a later received higher priority interrupt permitted by the dynamically alterable interrupt mask. However, this is wholly unlike the video apparatus having a digital decoder and method for controlling the video apparatus as claimed in claims 1 and 6 of the present invention.

Specifically, Cottle et al. disclose in Figure 1b that the receiver comprises an SDRAM 312 which is used to store OSD data prepared by processor 220 for access by OSD circuit 270 as well as demultiplexed Transport Stream (TS) data provided by a Transport Packet. Cottle et al. further disclose that parser 210 accesses the A/V core 250, and decoded and decompressed video provided by the A/V core is accessible by the OSD and Digital video circuit 270 for combination with OSD data. Cottle et al. further provide for an external memory 300-1 which is accessible through extension bus 300 (see Figure 1B; column 7, line 52 – column 8, lines 19).

Cottle et al. further state in column 10, lines 6-23 that “[t]There may be limited space in the SDRAM 312 for OSD. Applications that require large quantities of OSD data preferably store them in an external memory attached to the expansion bus.” However, Cottle et al. neither disclose nor suggests the type of ‘OSD data’ and whether any transfer of the OSD data is to occur from memory to memory. Therefore, Cottle et al. neither disclose nor suggest that “the first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and to transfer said on-screen display data back to the second memory in response to a request for display of data stored in the first memory” as in the present claimed invention. Thus, in the present claimed apparatus, the on-screen data which is not displayed any more is transferred to a “first memory” which is used for video decompression and is transferred back to the “second memory” which is the processor memory in response to

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a request to display the data. Cottle et al. does not disclose or suggest this kind of caching of OSD data.

In fact, Cottle et al. teaches away from the invention as claimed. Indeed any OSD data, be it stored in SDRAM 312 or an external RAM, can be transferred to the OSD circuit 270, either through a DMA from SDRAM 312, or through a double DMA, first from the external memory on the extension bus to the internal data memory 240 and then to the OSD circuit 270. So, even if OSD data were transferred from the SDRAM 312 to an external memory, which is neither disclosed nor suggested by Cottle et al., there is no indication nor any need that, upon request for display data, data from any external memory would be transferred back to the SDRAM.

Furthermore, Cottle et al. neither disclose nor suggest “a processing unit, wherein the first memory not being directly accessible by the processing unit” as claimed in claim 2 of the present invention. Specifically, as stated above regarding the rejection to claim 1, the memory units are both accessible by the processor 220 as clearly shown in Figure 1B of Cottle et al. Thus, as the processor is able to access “the first memory...and the second memory” the circuit disclosed by Cottle et al. is not equivalent to the circuit as claimed in claim 2 of the present invention.

Additionally, Cottle et al. neither disclose nor suggest the “process of controlling a video apparatus comprising a digital decoder...comprising the steps of writing on-screen display data to the second memory for access by the on-screen display circuit; wherein, the first memory is used for video decompression” as claimed in claim 6 of the present invention. Cottle et al. also neither disclose nor suggest “transferring on-screen display data that is no longer being be displayed to the first memory; and upon request, transferring back on-screen display data from the first memory to the second memory” as claimed in claim 6 of the present invention.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Cottle et al. that anticipates the present invention as claimed in claims 1 and 6. As claims 2, 4 – 5 and

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10 – 11 are dependent on claim 1 and as claims 7 – 9 are dependent on claim 6, it is respectfully submitted that claims 2, 4 – 5 and 7 – 11 are also not anticipated by Cottle et al. for the reasons discussed above with respect to claims 1 and 6. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Applicants respectfully submit that new claims 9 – 11 are also not anticipated by Cottle et al. as they are dependent upon either independent claim 1 or independent claim 6. Applicants further respectfully submit that Cottle et al. neither discloses nor suggests that “the transfer of on-screen display data to the first memory occurs when the first memory is unavailable for video decompression” as claimed in claim 9 of the present invention. Additionally, Cottle et al. neither disclose nor suggest that “the first memory is made available for storing on-screen display where the first memory is not being used for holding video data” as claimed in claim 11 of the present invention.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicants' attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Please charge the \$450 fee for the 2 month Petition for Extension of Time, and any other cost that may be associated with the filing of this response, to Deposit Account No. 07-0832.

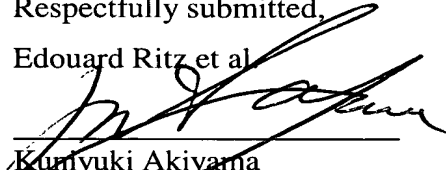
Thomson Licensing Inc.  
Patent Operations  
P.O. Box 5312  
Princeton, NJ 08543-5312

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Respectfully submitted,

Edouard Ritz et al.

By:

  
Kunyuki Akiyama  
Registration No.: 43,314  
(609) 734-6801